**SRMIST**

**Department of ECE**

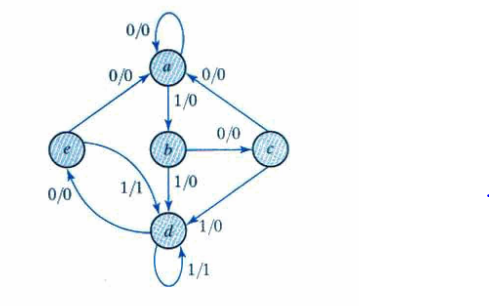
**Academic year 2022-23(Even sem)**

**Subject:18ECC206J - VLSI Design Semester: VI**

**Unit 1:**

**Assignment-1 (Any two from Q.No 1 to 3)**

1. Using Verilog code Design a 6-bit counter. The counter starts counting at count = 5 and finishes at count = 60. The count is incremented at positive edge of clock.
2. Write and verify Verilog behavioral descriptions of the state machines shown in Fig.



1. Answer the following questions.

A. Write the output for the following expression.

a=0111, b=1100, c=0100, x=5, y=10;

f1=~a | b;

f2=(a & ~b)|(b & c & ~d);

f3=(x==y)?x+2:x-2;

B. Write the Verilog code for the Circuit shown below.

Diagram

Description automatically generated

c. With the help of Verilog code design a combinational circuit with data inputs D0, D1, D2 & D3 and two selection lines S0 & S1 and one output Y. One of these 4 inputs will be connected to the output based on the combination of inputs present at these two selection lines. Truth table of the circuit is shown below.

